texture buffer having decompressed texture data. The processor reads the compressed texture data from the storage device and decompresses the texture data. The processor then stores the decompressed texture data in the texture buffer.

IN THE DRAWINGS:

Please amend the drawings as in the attached Request For Approval of Drawing Corrections.

IN THE CLAIMS:

Please cancel claims 1-9 without prejudice or disclaimer of the subject matter contained therein.

Please add the following new claims:

--10. An apparatus for image processing, comprising:

a processor including a data decompression circuit;

a first storage device having texture data and electronically coupled to said processor; and

a texture buffer having decompressed texture data and electronically coupled to said processor.

11. The apparatus of claim 10, further comprising a frame buffer, wherein said processor stores image data in said frame buffer.

12. The apparatus of claim 10, wherein said processor reads decompressed texture data contained in said texture buffer and performs image processing of said decompressed texture data for conversion to image data.

13. The apparatus of claim 10, wherein said processor reads compressed texture data from said first storage device, said data decompression circuit decompresses said read compressed texture data, and said processor stores said decompressed texture data in said texture buffer.

14. The apparatus of claim 10, wherein transmission of texture data between said texture buffer and said processor is faster than transmission of texture data between said storage device and said processor.

15. The apparatus of claim 10, further comprising a first data bus and a second data bus, wherein said first data bus carries texture data between said texture buffer and said processor faster than said second bus carries texture data from said storage device and said processor.

16. The apparatus of Claim 13, wherein said processor includes a FIFO storage device which temporarily stores said read compressed texture data.

17. The apparatus of Claim 16, wherein said data decompression circuit receives said read compressed texture data from said FIFO storage device.

18. The apparatus of Claim 13, wherein said processor includes a palette transformation circuit, said palette transformation circuit performing palette transformation of said decompressed texture data.

19. The apparatus of Claim 13, wherein said processor includes a mip map generation circuit, said mip map generation circuit generating a mip map of said decompressed texture data.

20. The apparatus of claim 10, wherein said texture data in said first storage device is compressed.

21. An image processing method comprising the steps of:

providing compressed texture data in a storage device;

reading said compressed texture data from said storage device and decompressing said compressed texture data; and

storing said decompressed texture data in a texture buffer.

22. The method of claim 21, further comprising the step of converting said decompressed texture data to image data, and storing said image data in a frame buffer.

23. The method of claim 21, further comprising the step of providing a processor, and transferring data between said texture buffer and said processor faster than transferring data between said storage device and said processor.

24. The method of claim 21, further comprising the step of performing palette conversion of said decompressed texture data prior to said step of storing said texture data.

25. The method of Claim 21, further comprising the step of generating a mip map of said decompressed texture data prior to said step of storing said decompressed texture data.

26. The method of claim 21, wherein said step of storing said decompressed texture data includes the step of updating said decompressed texture data in said texture buffer with new decompressed texture data.--